Abstract

A design which allows burn-in of DRAM's at the wafer level, as opposed to in die form or after the package has been assembled. The DRAM dies on the wafer are IEE1149.1 (JTAG) compliant, and the TDO pad of each die is connected to the TDI pad of the next die. The dies are arranged in rows, and each die in a given row is daisy chained to the next die in the row. The last die in the row is daisy chained to the first die in the next row. Additionally, the TMS and TCK pads of the dies are connected in parallel, such as via metal lines running along the scribe area of the wafer. The DRAM dies on the wafer are also connected to power busses along the scribe area so that the individual dies can be powered.